AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

In the claims

Claim 1 (currently amended): A computer system comprising:

(A) a CPU (central processor unit);

(B) a memory arrangement comprising:

(i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion;

(ii) a charge pump for providing a voltage to accumulate negative charges in the side-wall portion of each side-wall memory transistor during a programming operation;

(iii) a plurality of switching circuits each coupled to the charge pump for receiving the voltage provided by the charge pump and for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and

(iv) logic circuitry for enabling the plurality of switching circuits in a selected sequential order; and

(C) a system bus for transferring data and addresses between the CPU and the memory arrangement,

wherein each of the side-wall memory transistors comprises:

only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer;

a channel region formed below the gate electrode;

a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and

a pair of memory functional units formed on ~~the~~ both sides of the gate electrode and having a function of retaining charges wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed

independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

Claim 2 (original): The computer system of claim 1, wherein the side-wall memory transistors are in sets and wherein the plurality of switching circuits are connected to the sets of bitlines, and a switching circuit of the plurality of switching circuits is enabled to transfer a first voltage to a selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed.

Claim 3 (original): The computer system of claim 1, wherein the logic circuitry comprises a state machine, the state machine enabling the plurality of switching circuits in a selected sequential order such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed.

Claim 4 (original): The computer system of claim 3, further comprising a bit line select circuit coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed.

Claim 5 (original): The computer system of claim 1, wherein each of the sets includes four bitlines.

Claim 6 (original): The computer system of claim 1, wherein the plurality of switching circuits comprise four switching circuits, each switching circuit is coupled to a corresponding set of four bitlines.

Claim 7 (original): The computer system of claim 1, the plurality of switching circuits for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array

comprise four switching circuits, a switching circuit is coupled to a corresponding set of four bitlines.

Claim 8 (currently amended): A memory structure comprising:

(i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion;

(ii) a charge pump for providing a voltage to accumulate negative charges in the side-wall portion of each side-wall memory transistor during a programming operation;

(iii) a plurality of switching circuits each coupled to the charge pump for receiving the voltage provided by the charge pump and for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and

(iv) logic circuitry for enabling the plurality of switching circuits in a selected sequential order,

wherein each of the side-wall memory transistors comprises:

only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer;

a channel region formed below the gate electrode;

a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and

a pair of memory functional units formed on ~~the~~ both sides of the gate electrode and having a function of retaining charges wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

Claim 9 (original): The memory structure of claim 8, wherein the side-wall memory transistors are in sets and wherein the plurality of switching circuits are connected to the sets of bitlines, and a switching circuit of the plurality of switching circuits is enabled to transfer a first voltage to a selected set of the sets of bitlines being coupled to a set of the sets of side-wall memory

transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed.

Claim 10 (original): The memory structure of claim 8, wherein the logic circuitry comprises a state machine, the state machine enabling the plurality of switching circuits in a selected sequential order such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed.

Claim 11 (original): The memory structure of claim 10, further comprising a bit line select circuit coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed.

Claim 12 (original): The memory structure of claim 8, wherein each of the sets includes four bitlines.

Claim 13 (original): The memory structure of claim 8, wherein the plurality of switching circuits comprise four switching circuits, each switching circuit is coupled to a corresponding set of four bitlines.

Claim 14 (currently amended): A computer system comprising:

(A) central processing means;

(B) means for providing storage of data comprising:

(i) side-wall memory array means including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion;

(ii) charge pump means for providing a voltage to accumulate negative charges in the side-wall portion of each side-wall memory transistor during a programming operation;

(iii) a plurality of means for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and

(iv) means for enabling the plurality of transferring means in a selected sequential order; and

(C) a system bus means for transferring data and addresses between the central processing means and the means for providing storage of data,

wherein each of the side-wall memory transistors comprises:

only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer;

a channel region formed below the gate electrode;

a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and

a pair of memory functional units formed on ~~the~~ both sides of the gate electrode and having a function of retaining charges wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

Claim 15 (original): The computer system of claim 14, wherein the side-wall memory transistors are in sets and wherein selected transferring means of the plurality of transferring means is connected to a selected set of the sets of bitlines, and is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed.

Claim 16 (original): The computer system of claim 14, wherein the enabling means comprises a state machine, the state machine enabling each of the transferring means such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed.

Claim 17 (original): The computer system of claim 14, wherein each of the sets includes four bitlines.

Claim 18 (original): The computer system of claim 14, wherein the plurality of transferring means comprise four switching circuits.

Claim 19 (currently amended): A structure for providing storage of data, comprising:

(i) side-wall memory array means including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion;

(ii) charge pump means for providing a voltage to accumulate negative charges in the side-wall portion of each side-wall memory transistor during a programming operation;

(iii) a plurality of means for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and

(iv) means for enabling the plurality of transferring means in a selected sequential order, wherein each of the side-wall memory transistors comprises:

only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer;

a channel region formed below the gate electrode;

a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and

a pair of memory functional units formed on ~~the~~ both sides of the gate electrode and having a function of retaining charges wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

Claim 20 (currently amended): The structure for ~~proving~~ providing storage of data of claim 19, wherein the side-wall memory transistors are in sets and wherein the plurality of transferring means are connected to the sets of bitlines, and transferring means of the plurality of transferring

means is enabled to transfer a first voltage to a selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed.

Claim 21 (currently amended): The structure for ~~proving~~ providing storage of data of claim 19, wherein the enabling means comprises a state machine, the state machine enabling the plurality of transferring means such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed.

Claim 22 (currently amended): The structure for ~~proving~~ providing storage of data of claim 19, wherein each of the sets includes four bitlines.

Claim 23 (currently amended): The structure for ~~proving~~ providing storage of data of claim 19, the plurality of means for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four switching circuits, a switching circuit is coupled to a corresponding set of four bitlines.

Claim 24 (new): The system of either claim 1 or claim 14 wherein the pair of diffusion regions are disposed so as to offset with an end of the gate electrode.

Claim 25 (new): The system of either claim 1 or claim 14 wherein the diffusion region is disposed so as to overlap with the memory functional element.

Claim 26 (new): The system of either claim 1 or claim 14 wherein an overlap amount between the memory functional element and the diffusion region is 10 nm or more.

Claim 27 (new): The system of either claim 1 or claim 14 wherein a distance between an end of the gate electrode and an end of the diffusion region on the channel region side is less than 100 nm.

Claim 28 (new): The system of either claim 1 or claim 14 wherein the memory functional element is formed by at least any one of an insulating film including an insulator having the function of retaining charges, an insulating film including at least one conductor or semiconductor dot, and an insulating film including a ferroelectric film of which inner charge is polarized by an electric field and in which the polarized state is held.

Claim 29 (new): The structure of either claim 8 or claim 19 wherein the pair of diffusion regions are disposed so as to offset with an end of the gate electrode.

Claim 30 (new): The structure of either claim 8 or claim 19 wherein the diffusion region is disposed so as to overlap with the memory functional element.

Claim 31 (new): The structure of either claim 8 or claim 19 wherein an overlap amount between the memory functional element and the diffusion region is 10 nm or more.

Claim 32 (new): The structure of either claim 8 or claim 19 wherein a distance between an end of the gate electrode and an end of the diffusion region on the channel region side is less than 100 nm.

Claim 33 (new): The structure of either claim 8 or claim 19 wherein the memory functional element is formed by at least any one of an insulating film including an insulator having the function of retaining charges, an insulating film including at least one conductor or semiconductor dot, and an insulating film including a ferroelectric film of which inner charge is polarized by an electric field and in which the polarized state is held.